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On April 20, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Andrea

PATENT
Attorney Docket No.: A1126/T08910
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:

KRAMADHATI V. RAVI et al.

Application No.: 09/362,504

Filed: July 27, 1999

For: METHOD FOR REDUCING THE INTRINSIC STRESS OF HIGH DENSITY PLASMA FILMS

Examiner: Rudy Zervigon

Art Unit: 1763

APPELLANT'S BRIEF UNDER 37 CFR § 1.192

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants, in the above-captioned patent application, appeal the final rejection of claims 16-36. The claims on appeal have been finally rejected pursuant to MPEP § 706.07(b). Accordingly, this appeal is believed to be proper. This appeal brief is filed in triplicate.

I. REAL PARTY IN INTEREST:

The real party in interest for the above-identified application is APPLIED MATERIALS, INC., a Delaware corporation having its principal place of business at P.O. Box 450A, Santa Clara, California 95052. The assignment is recorded in the U.S. Patent and Trademark Office on October 16, 1996 at Reel 8331/Frame 0398.

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II. RELATED APPEALS AND INTERFERENCES:

There are no appeals or interferences related to the present appeal.

III. STATUS OF CLAIMS:

Claims 16-36 are pending.

Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al. Claims 17, 18, 25-28, and 32-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al. Claims 19-24, 29-31, 35, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura.

Applicants note that claim 28 depends from claim 30. Claim 28, however, stands rejected over the same references upon which claim 30 is rejected but without Matsuura. This appears inconsistent. Claim 30 depends from claim 17, and recites that the plasma generating system includes a first electrode, a second electrode, and a coil disposed about the vacuum chamber, wherein the pedestal includes the second electrode. Claim 28 depends from claim 30, and recites that the substrate is disposed on the second electrode and electric energy is applied to the first and second electrodes while maintaining the application of the RF energy. Matsuura is cited for allegedly disclosing a method of forming silicon and oxygen combined thin films for superior crack resistance and insulation by optionally applying silane and oxygen gases, which is not related to the limitations of claims 30 and 28. For purposes of this appeal, however, Applicants will address the rejections as stated by the Examiner, even though they are inconsistent.

IV. STATUS OF AMENDMENTS:

Claim 16 was rejected under 35 U.S.C. § 102(b) and claims 17-36 were rejected under 35 U.S.C. § 103(a) upon the grounds set forth in the Final Office Action mailed on June 27, 2000.

As stated in the Interview Summary dated August 9, 2000, a telephonic interview was conducted between the Examiner and Applicants' counsel, Chun-Pok Leung. An agreement was reached as follows: "Reference was made to the Figure 1 waveforms of the Jin Onuki et al reference which shows a cycling of power application and substrate biasing. In view of claim 16, Mr. Leung suggested claim language that I agreed would be suggestive

enough to remove a 102 rejection of the claim however would require a consideration under 103."

On August 25, 2000, Applicants filed a Continuation Prosecution Application with a Preliminary Amendment amending claims 16-18 and 32 as agreed upon during the telephonic interview.

On October 27, 2000, however, the Examiner issued a Final Office Action in response to the Preliminary Amendment. The Examiner apparently changed his mind, and maintained the rejection of claim 16 under 35 U.S.C. § 102(b) as well as the rejection of claims 17-36 under 35 U.S.C. § 103(a). Despite the agreed upon claim amendment, the Examiner made the action final by asserting that all the claims could have been finally rejected on the grounds and art of record in the next office action if they had been entered in the earlier application.

Applicants filed a Response to Office Action under 37 C.F.R. § 1.116 on December 15, 2000.

In an Advisory Action dated January 5, 2001, the Examiner maintained the rejection of all pending claims and stated: "It has been well demonstrated that Onuki et al teach the method limitations of claim 16 with reference to Fig. 1a,b. Fig. 1a,b teach both zero and non-zero bias voltages repeated between 1 and 18 cycles providing multiple layers (Section 2.1)."

In accordance with 37 C.F.R. § 1.192(c)(9), a copy of the claims involved in the appeal are contained in the Appendix attached hereto.

V. SUMMARY OF THE INVENTION:

Embodiments of the present invention provide a method and an apparatus for reducing the intrinsic stress of high density plasma (HDP) films by delaying or interrupting the application of capacitively coupled RF energy. This is accomplished by introducing a process gas into the HDP system chamber and forming a plasma from the process gas by the application of RF power to an inductive coil to deposit a first layer of the film. After a selected period, a second layer of the film is deposited by maintaining the inductively coupled plasma and biasing the plasma toward the substrate to enhance the sputtering effect of the plasma.

According to an embodiment of the present invention, an integrated circuit is formed on a semiconductor substrate by the method of flowing a process gas into a substrate processing chamber, and forming a plasma from the process gas by coupling sputtering energy into the substrate processing chamber. Thereafter, the plasma is maintained to deposit a first layer of a film over the substrate by sputtering without biasing the plasma toward the substrate. Thereafter, the plasma is maintained by maintaining coupling of the sputtering energy into the substrate processing chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer.

In accordance with another embodiment of the invention, an integrated circuit is formed on a semiconductor substrate, and comprises a plurality of active devices formed in the semiconductor substrate, and at least one metal layer formed above the semiconductor substrate. At least one insulating layer is formed between the metal layer and the semiconductor substrate. The insulating layer has a plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of the metal layer to selected portions of the semiconductor substrate. The insulating layer comprises a first silicon oxide layer and a second silicon oxide layer. The first and the second silicon oxide layers are deposited using a high-density plasma chemical vapor deposition process. The first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer.

VI. ISSUES:

The following issues are presented:

Whether claim 16 is properly rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al.

Whether claims 17, 18, 25-28, and 32-34 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al.

Whether claims 19-24, 29-31, 35, and 36 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura.

VII. GROUPING OF THE CLAIMS:

In the present case, the rejected claims do not all stand or fall together. Applicants submit that each claim presents distinct issues concerning patentability. In the interest of administrative economy and efficiency, however, Applicants agree to narrow the issues for the purposes of this appeal only by grouping the claims as follows:

Group 1: Claim 16, which relates generally to an integrated circuit formed by a method that forms a plasma from a process gas by coupling sputtering energy into a substrate processing chamber, wherein the method maintains the plasma to deposit a first layer of a film over the substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintains the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer;

Group 2: Claims 17, 25-28, and 30, which are directed generally to a substrate processing system including a memory for storing a program for directing the operation of the system, wherein the program includes a set of instructions for depositing a film by controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into the chamber and deposit a first layer of the film over the substrate by sputtering without biasing the plasma towards the substrates, and controlling the plasma generation system to maintain the plasma by maintaining coupling of the sputtering energy into the chamber and bias the plasma toward the substrate to deposit a second layer of the film over the first layer;

Group 3: Claim 18, which is directed generally to the same subject matter as claim 17, but which includes the additional limitation that the program includes instructions for depositing a plurality of the first layers and second layers until the desired thickness of the film is reached;

Group 4: Claims 19, 29, and 31, which are directed generally to the same subject matter as claim 17, but which include the additional limitation that the process gas includes silicon and oxygen;

Group 5: Claims 20-22, which relate generally to a high-density plasma chemical vapor deposition system, wherein the apparatus includes means for generating a plasma from reactants by applying a sputtering power to the reactants to deposit a first layer of a film on the substrate during a first time period, and means for biasing the plasma toward the substrate during a second time period after the first time period to enhance a sputtering of the plasma while maintaining application of the sputtering power to the reactants and deposit the subsequent layer.

Group 6: Claim 23, which relates generally to an integrated circuit including a plurality of active devices formed in the substrate, at least one metal layer formed above the substrate, and at least one insulating layer formed between the metal layer and the substrate, wherein the insulating layer has a plurality of patterned hoes filled with electrically conductive material to electrically connect selected portions of the metal layer to selected portions of the semiconductor substrate, wherein the insulating layer comprises a first silicon oxide layer and a second silicon oxide layer, and wherein the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer;

Group 7: Claim 24, which is directed generally to the same subject matter as claim 23, but which includes the additional limitation that the a second metal layer is formed above the substrate and below the at least one insulating layer, and a second insulating layer is formed between the second metal layer and the substrate;

Group 8: Claim 36, which is directed generally to the same subject matter as claim 23, but which includes the additional limitation that the first silicon oxide layer is deposited on the substrate by applying a sputtering power to reactants to generate a plasma in a process chamber, and the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants;

Group 9: Claims 32-34, which relate generally to a computer readable storage medium having a program code controlling a semiconductor processing system to

process a wafer in a chamber, wherein the program code includes instructions for controlling the plasma generating system to form a plasma from the process gas by coupling sputtering energy into the processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing the plasma towards the substrate, and instructions for controlling the plasma generation system to maintain the plasma by maintaining coupling of the sputtering energy into the processing chamber and to bias the plasma toward the substrate to deposit a second layer of the film over the first layer; and

Group 10: Claim 35, which is directed generally to the same subject matter as claim 32, but which includes the additional limitation that the process gas includes silicon and oxygen.

VIII. DISCUSSION OF THE REFERENCES RELIED UPON BY THE EXAMINER:

In rejecting the claims under 35 U.S.C. §§ 102(b) and 103(a), the Examiner relied upon the following references:

1. Ye et al. (United States Patent No. 5,710,486)

Ye et al. discloses a plasma reactor for processing a semiconductor wafer. The reactor includes a pair of parallel capacitive electrodes at the ceiling and base of the processing chamber, respectively. Each capacitive electrode capacitively couples RF power into the chamber. An inductive coil is wound around a portion of the chamber and inductively couples RF power into the chamber.

2. Onuki et al.

Onuki et al. discloses a switching bias sputtering process whereby d.c. sputtering and d.c. bias sputtering are operated alternately (page 182, right column, lines 9-11). As illustrated in Figs 1 and 2, the switching bias sputtering process involves alternating step pulses of sputtering power and bias voltage. The step pulses of sputtering power and bias voltage alternate, and do not overlap in time. The use of the switching bias sputtering method is intended to enhance the step coverage and quality of Al films (page 182, right column, lines 12-13).

3. Boys et al. (United States Patent No. 4,500,408)

Boys et al. discloses a magnetron sputter coating apparatus having a magnetic field which is controlled in response to measurements of plasma parameters to control deposition parameters, such as sputter deposition rate and material deposition thickness profile.

4. Ramarotafika et al.

Ramarotafika et al. describes the influence of d.c. substrate bias on the resistivity, composition, crystallite size, and microstrain of WTi and WTi-N films deposited by r.f. magnetron sputtering.

5. Matsuura (United States Patent No. 5,319,247)

Matsuura discloses silicon oxide films in a semiconductor device allegedly having superior crack resistance, superior step coverage, and superior recess-filling characteristics (col. 3, lines 17-32 and Abstract). The semiconductor device includes a first silicon oxide film formed on a semiconductor substrate to cover the surface of a stepped pattern, a second silicon oxide film deposited on the first film to fill the recessed portions of the stepped pattern, a third silicon oxide film placed into the recessed portions on the surface of the second film after its etching, and a fourth silicon oxide film formed on the substrate including the second and third silicon oxide films.

IX. ARGUMENTS:

Because all the claims do not stand or fall together, Applicants will present arguments for each claim group.

In rejecting the claims, the Examiner relies on Onuki et al. for allegedly disclosing maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al., however, specifically discloses terminating the sputtering power during application of the bias voltage.

The Examiner points to Fig. 1(a) in Onuki et al. for the disclosure of maintaining the application of the sputtering power while biasing the plasma toward the substrate. In the Advisory Action dated January 5, 2001, the Examiner asserts: "It has been

well demonstrated that Onuki et al teach the method limitations of claim 16 with reference to Fig. 1a,b. Fig. 1a,b teach both zero and non-zero bias voltages repeated between 1 and 18 cycles providing multiple layers (Section 2.1)."

Fig. 1b clearly shows **no** overlap between the bias voltage and the sputtering power. Fig. 1a merely shows a conventional DC sputtering with 4kW sputtering power and zero bias voltage, and conventional DC bias sputtering with 4kW sputtering power and –200V bias voltage. Nothing in Onuki et al., however, teaches or suggests combining or alternating the conventional DC sputtering and DC bias sputtering. As to the 18 cycles mentioned in the Examiner's statement, Onuki et al. actually states: "In the case of one-step switching bias sputtering, a cycle consisted of 5 s d.c. and 5 s d.c. bias sputtering. A cycle was repeated 18 times for the formation of 0.5 μm thick Al-0.5wt.%Cu-1wt.%Si films." This relates to the one-step switching bias sputtering shown in Fig. 1b in which there is **no** overlap between the sputtering power and the bias voltage. It has nothing to do with the conventional DC sputtering and conventional DC bias sputtering shown in Fig. 1a. Clearly, the Examiner has misconstrued Onuki et al.

Claim Group 1

Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al. To sustain a Section 102(b) rejection, the Examiner must establish that the reference discloses every element of the claim. In this case, **Onuki et al. does not disclose or suggest every element of claim 16.**

Onuki et al. discloses a switching bias sputtering process whereby d.c. sputtering and d.c. bias sputtering are operated alternately (page 182, right column, lines 9-11). As illustrated in Figs. 1 and 2, the switching bias sputtering process involves alternating step pulses of sputtering power and bias voltage. The step pulses of sputtering power and bias voltage alternate, and do not overlap in time. The use of the switching bias sputtering method is intended to enhance the step coverage and quality of Al films (page 182, right column, lines 12-13).

As discussed above, Onuki et al. does not disclose or suggest maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and,

thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage.

The Examiner misconstrues Onuki et al., including the teachings of Fig. 1a,b, to arrive at the erroneous conclusion that Onuki et al. anticipates claim 16. Claim 16 recites depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. Onuki et al. clearly does not teach depositing the two different layers. Nor does Onuki et al. recognize that the first layer formed without biasing the plasma is a reduced stress layer for reducing the stress of films deposited on the substrate (Page 4, lines 1-3 and Abstract). Therefore, claim 16 is novel and patentable over Onuki et al.

Claim Group 2

Claims 17 and 25-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al. Claim 30 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura.

The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

The remaining references do not cure the defects of Ye et al. and Onuki et al. The Examiner cites Boys et al. merely for allegedly disclosing a programmable memory controller for controlling a plasma deposition system. Ramarotafika et al. describes the influence of d.c. substrate bias on the resistivity, composition, crystallite size, and microstrain

of WTi and WTi-N films. Matsuura discloses silicon oxide films in a semiconductor device allegedly having superior crack resistance, superior step coverage, and superior recess-filling characteristics (col. 3, lines 17-32 and Abstract). None of them teach or suggest depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. The references are directed to very different processes for forming different films to achieve different purposes. For example, Onuki et al. is directed to forming sputtered Al and Al alloy films using switching bias sputtering involving d.c. sputtering and d.c. bias sputtering; Ramarotafika et al. is directed to forming WTi and WTi-N films by r.f. magnetron sputtering with d.c. substrate bias; and Matsuura relates to deposition of silicon oxide films by plasma CVD. There is no suggestion that the operating conditions for depositing silicon oxide layers in Matsuura can be combined with the switching bias sputtering technique taught in Onuki et al. For at least the foregoing reasons, Applicants respectfully submit that claim 17 and claims 25-28 and 30 depending therefrom are patentable.

Claim Group 3

Claim 18 stands rejected on the same grounds as claim 17 from which claim 18 depends. Applicants believe claim 18 is allowable for the same reasons that claim 17 is allowable. Claim 18 further recites that the program includes instructions for depositing a plurality of the first layers and second layers until the desired thickness of the film is reached. The references do not disclose or suggest depositing a plurality of first layers by sputtering without biasing the plasma and second layers by sputtering and biasing the plasma. Matsuura merely discloses formation of silicon oxide films, and does not cure the defects of the other references. Therefore, claim 18 is patentable.

Claim Group 4

Claims 19, 29, and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Claims 19 and 29 depend from claim 17 and further recite silicon and oxygen in the process gas. Claim 31 depends from claim 19 and recites that the silicon source contains silane. Applicants believe claims 19, 29, and 31 are patentable for at least the same reasons

that claim 17 is patentable. For instance, the references do not teach or suggest depositing a first layer by sputtering without biasing the plasma and a second layer by sputtering and biasing the plasma generated from a process gas having silicon and oxygen. Matsuura merely discloses formation of silicon oxide films, and does not cure the defects of the other references. Therefore, claims 19, 29, and 31 are patentable.

Claim Group 5

Claims 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. The remaining references do not cure the defects of Ye et al. and Onuki et al. Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. Accordingly, claims 20-22 are patentable.

Claim Group 6

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Applicants respectfully assert that these claims are patentable over the references because, for instance, the references do not teach or suggest an insulating layer formed between the metal layer and the semiconductor substrate and including a first silicon oxide layer and a second silicon oxide layer deposited using a high-density plasma chemical vapor deposition process, where the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer.

Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness, since the Examiner has not pointed to anything in the references that would suggest the claimed invention. Neither Onuki et al. nor Ramarotafika et al. teach depositing silicon oxide layers. Matsuura discloses silicon oxide layers, but fails to teach or suggest a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer. For at least the foregoing reasons, Applicants respectfully submit that claim 23 is patentable.

Claim Group 7

Claim 24 stands rejected on the same grounds as claim 23 from which claim 24 depends. Applicants believe that claim 24 is allowable for the same reasons that claim 23 is allowable. Further, claim 24 recites that a second metal layer is formed above the substrate and below the at least one insulating layer, and a second insulating layer is formed between the second metal layer and the substrate. These features are also missing from the references. Thus, claim 24 is patentable.

Claim Group 8

Claim 36 stands rejected on the same grounds as claim 23 from which claim 36 depends. Applicants believe that claim 36 is allowable for the same reasons that claim 23 is allowable. Further, claim 36 recites that the first silicon oxide layer is deposited on the substrate by applying a sputtering power to reactants to generate a plasma in a process chamber, and the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants.

As discussed above, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. The remaining references do not cure the defects of Onuki et al. Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. Accordingly, claim 36 is patentable.

Claim Group 9

Claims 32-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al.

The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. The remaining references do not cure the defects of Ye et al. and Onuki et al. Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. For at least the foregoing reasons, Applicants respectfully submit that claims 32-34 are patentable.

Claim Group 10

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Claim 35 depends from claim 32 and is submitted to be patentable for at least the same reasons that claim 32 is patentable as discussed above. Matsuura merely discloses formation of silicon oxide films, and does not cure the defects of the other references. Therefore, claim 35 is patentable.

X. CONCLUSION:

In view of the foregoing arguments distinguishing claims 16-36 over the art of record, Applicants respectfully submit that the claims are in condition for allowance, and respectfully request that the rejection of these claims be reversed.

Respectfully submitted,

Chun-Pok Leung
Reg. No. 41,405

TOWNSEND and TOWNSEND and CREW LLP
Tel: (415) 576-0200
Fax: (415) 576-0300
RL
PA 3130928 v1

Encl.: Appendix of claims involved in appeal

APPENDIX

16. An integrated circuit formed on a semiconductor substrate by the method of:

a) flowing a process gas into a substrate processing chamber;

b) forming a plasma from said process gas by coupling sputtering energy into said substrate processing chamber;

c) thereafter, maintaining said plasma to deposit a first layer of a film over said substrate by sputtering without biasing said plasma toward said substrate; and

d) thereafter, maintaining said plasma by maintaining coupling of said sputtering energy into said substrate processing chamber and biasing said plasma toward said substrate to deposit a second layer of said film over said first layer.

17. A substrate processing system comprising:

a housing for forming a vacuum chamber;

a vacuum pump for evacuating said vacuum chamber;

a pedestal, located within said housing, configured to hold a substrate;

a gas distribution system fluidly coupled to said vacuum chamber;

a plasma generation system for forming a plasma from process gas within said vacuum chamber and for selectively biasing said plasma toward said substrate;

a controller for controlling said vacuum pump, said gas distribution system and said plasma generation system;

a memory coupled to said controller and storing a program for directing the operation of said system, said program including a set of instructions for depositing a film by

first, controlling said gas distribution system to introduce said process gas into said chamber;

second, controlling said plasma generation system to form a plasma from said process gas by coupling sputtering energy into said vacuum chamber and deposit a first layer of said film over said substrate by sputtering without biasing said plasma towards said substrate; and

third, controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

18. The substrate processing system of claim 17 wherein said program further includes instructions for depositing a plurality of said first layers and said second layers by

fourth, depositing a third layer of said film over said second layer by controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and stop biasing said plasma toward said substrate;

fifth, depositing a fourth layer of said film over said third layer by controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said vacuum chamber and bias said plasma toward said substrate; and

sixth, performing the second and third steps iteratively at least once until a desired thickness of said film is reached.

19. The apparatus of claim 17 wherein said gas distribution system includes sources of silicon and oxygen fluidly coupled to said gas distribution system.

20. A high-density plasma chemical vapor deposition system comprising:

a housing for forming a vacuum chamber;

a pedestal, located within said housing, for holding a substrate;

means for introducing reactants into said vacuum chamber;

means for generating a plasma from said reactants by applying a sputtering power to said reactants to deposit a first layer of a film on said substrate during a first time period, said first layer for the reduction of mechanical stress in a subsequently deposited layer of a silicon oxide film; and

means for biasing said plasma toward said substrate during a second time period after said first time period to enhance a sputtering of said plasma while maintaining application of said sputtering power to said reactants and deposit said subsequent layer.

21. The apparatus of claim 20, further comprising means for maintaining a pressure of between about 0.001-10 torr in said vacuum chamber while said films are deposited.

22. The apparatus of claim 20, further comprising means for maintaining a wafer temperature of between about 100-500°C in said vacuum chamber while said films are deposited.

23. An integrated circuit formed on a semiconductor substrate, said integrated circuit comprising:

(a) a plurality of active devices formed in said semiconductor substrate;

(b) at least one metal layer formed above said semiconductor substrate; and

(c) at least one insulating layer formed between said metal layer and said semiconductor substrate, said insulating layer having a plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of said metal layer to selected portions of said semiconductor substrate, wherein said insulating layer comprises a first silicon oxide layer and a second silicon oxide layer, said first and said second silicon oxide layers deposited using a high-density plasma chemical vapor deposition process, said first silicon oxide layer deposited for the reduction of mechanical stress in said second silicon oxide layer.

24. The integrated circuit of claim 23, further comprising:

(d) a second metal layer formed above said semiconductor substrate and below said at least one insulating layer;

(e) a second insulating layer formed between said second metal layer and said semiconductor substrate, said second insulating layer having a second plurality of patterned holes filled with electrically conductive material to electrically connect selected portions of said second metal layer to selected areas of said plurality of active devices.

25. The substrate processing system of claim 17 wherein said plasma is an inductively coupled plasma.

26. The substrate processing system of claim 25 wherein said inductively coupled plasma is formed from said process gas using only RF energy applied to a coil disposed about the processing chamber.

27. The substrate processing system of claim 25 wherein said substrate processing chamber is a high-density plasma chemical vapor deposition chamber and said inductively coupled plasma is a high density plasma.

28. The substrate processing system of claim 30 wherein the substrate is disposed on said second electrode and electric energy is applied to said first and second electrodes while maintaining the application of said RF energy.

29. The substrate processing system of claim 17 wherein said process gas introduced by said gas distribution system includes flows of silicon and oxygen.

30. The processing system of claim 17 wherein said plasma generating system includes a first electrode, a second electrode, and a coil disposed about the vacuum chamber, wherein said pedestal includes said second electrode.

31. The substrate processing system of claim 19 wherein said source of silicon contains silane.

32. A computer readable storage medium having program code embodied therein, said program code for controlling a substrate processing system, wherein said substrate processing system includes a processing chamber, a gas delivery system, a plasma generation system and a controller configured to control the gas delivery system and the plasma generation system said program code controlling the semiconductor processing system to process a wafer in the chamber in accordance with the following:

(i) a first set of computer instructions for controlling the gas delivery system to introduce a process gas into the processing chamber;

(ii) a second set of computer instructions for controlling the plasma generation system to form a plasma from the process gas by coupling sputtering energy into said processing chamber to deposit a first layer of a film over a substrate by sputtering without biasing said plasma towards said substrate; and

(iii) a third set of computer instructions for controlling said plasma generation system to maintain said plasma by maintaining coupling of said sputtering energy into said processing chamber and to bias said plasma toward said substrate to deposit a second layer of said film over said first layer.

33. The computer readable storage medium of claim 32, wherein said plasma is an inductively coupled plasma.

34. The computer readable storage medium of claim 33 wherein said substrate processing system is a high density plasma system.

35. The computer readable storage medium of claim 32 wherein said process gas includes flows of silicon and oxygen.

36. The integrated circuit of claim 23 wherein the first silicon oxide layer is deposited on the substrate by placing the substrate in a process chamber and applying a sputtering power to reactants to generate a plasma in the process chamber, and wherein the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants.